What is claimed is:

1. A method of transmitting data over a source synchronous communications interface, the method comprising:

(a) receiving a source synchronous data strobe signal driven by a data source during a data transfer from the data source; and

(b) disabling a data latch from latching data received from the data source whenever the data source is not driving the source synchronous data strobe signal.

2. The method of claim 1, wherein disabling the data latch comprises gating the source synchronous data strobe signal.

3. The method of claim 2, wherein gating the source synchronous data strobe signal comprises applying a gate signal to the data latch that enables latching by the data latch only when the gate signal is asserted, wherein the gate signal is asserted proximate a start of a data transfer from the data source, and deasserted proximate an end of the data transfer from the data source.

4. The method of claim 3, wherein applying the gate signal comprises asserting the gate signal responsive to a synchronous enable signal that is asserted proximate the start of the data transfer from the data source.

5. The method of claim 4, wherein applying the gate signal further comprises deasserting the gate signal responsive to a synchronous postamble signal that is asserted proximate the end of the data transfer from the data source.

6. The method of claim 1, further comprising locally tracking progress of the data transfer from the data source.

7. The method of claim 6, wherein locally tracking the progress of the data transfer includes counting cycles of the source synchronous data strobe signal to track data transfer cycles during a data transfer from the data source.

8. The method of claim 7, wherein locally tracking the progress of the data transfer further includes indicating whenever the number of data transfer cycles is equivalent to a burst length for the data transfer.

9. The method of claim 1, wherein the data source comprises a synchronous dynamic random access memory (SDRAM), and wherein the source synchronous communications interface comprises an SDRAM memory interface.

10. The method of claim 9, wherein the data source comprises a double data rate (DDR) SDRAM, and wherein the source synchronous communications interface comprises a DDR SDRAM memory interface.

11. The method of claim 1, wherein gating the source synchronous data strobe signal comprises:

(a) incrementing a counter and outputting a burst length signal that indicates whether the counter stores a value equivalent to a predetermined burst length;

(b) performing a logical AND operation on the burst length signal and a synchronous postamble signal and outputting therefrom a first output signal, wherein the synchronous postamble signal is asserted proximate the end of a data transfer from the data source;

(c) performing a logical OR operation on the first output signal and a synchronous enable signal and outputting therefrom a gate signal, wherein the synchronous enable signal is asserted during the data transfer from the data source; and

(d) performing a logical AND operation on the gate signal and the source synchronous data strobe signal and outputting therefrom a gated source synchronous data strobe signal that is coupled to the data latch.

12. The method of claim 11, wherein incrementing the counter is performed in response to a logically-inverted gated source synchronous data strobe signal, and wherein the method further comprises logically-inverting the burst length signal prior to performing the logical AND operation.

13. The method of claim 1, wherein disabling the data latch comprises controlling a select input on a multiplexer coupled to an input of the data latch to select a first input among first and second inputs for the multiplexer, wherein the first input of the multiplexer is coupled to an output of the data latch, and the second input of the multiplexer is coupled to receive the data from the data source.

14. The method of claim 1, wherein the source synchronous data strobe signal comprises a DQS signal from a synchronous dynamic random access memory (SDRAM) during a transfer of read data from the SDRAM.

15. A method of transferring read data from a synchronous dynamic random access memory (SDRAM) over a source synchronous communications interface, the method comprising:

(a) receiving a source synchronous DQS signal driven by the SDRAM during a data transfer of read data from the SDRAM; and

(b) selectively disabling a data latch from latching data received from the SDRAM source whenever the SDRAM is not driving the DQS signal.